# Intel x86-64 Architecture

Version 1.02 [2011-12-19]

## General-purpose regs:

| | | | |
|---|---|---|---|
| RAX | EAX | AH | AL |
| | | AX | |
| RBX | EBX | BH | BL |
| | | BX | |
| RCX | ECX | CH | CL |
| | | CX | |
| RDX | EDX | DH | DL |
| | | DX | |
| RSI | ESI | | SIL |
| | | SI | |
| RDI | EDI | | DIL |
| | | DI | |

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## 64-bit mode registers:

| | | | |
|---|---|---|---|
| R8 | R8D | R8H | R8L |
| | | R8W | |
| ⋮ | | | |
| R15 | R15D | R15H | R15L |
| | | R15W | |

## Stack management:

| | | | |
|---|---|---|---|
| RSP | ESP | | SPL |
| | | SP | |
| RBP | EBP | | BPL |
| | | BP | |

## Flags register:

| | | |
|---|---|---|
| RFLAGS | EFLAGS | FLAGS |

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## Floating-point unit (FPU):

| | |
|---|---|
| ST7 | MM7 |
| ST6 | MM6 |
| ST5 | MM5 |
| ST4 | MM4 |
| ST3 | MM3 |
| ST2 | MM2 |
| ST1 | MM1 |
| ST0 | MM0 |

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tag | control | status

15 ... 0

opcode

last instr. pointer

last operand pointer

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## Segment registers:

| | |
|---|---|
| Code segment selector | CS |
| Data segment selector | DS |
| Stack segment selector | SS |
| Extra segment selector | ES |
| → **added with 80386:** | |
| Win32: access to KPCR/TIB | FS |
| Win64: access to KPCR/TIB | GS |

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## Control registers:

| | | |
|---|---|---|
| CR0 | CR1 | CR2 |
| sys control flags | reserved | page-fault addr |
| CR3 | CR4 | CR8 |
| PD base addr | processor ext. | task priority |
| | XCR0 | |
| | OS-supported extensions | |

## Debug registers:

| | | |
|---|---|---|
| DR0-3 | DR4 | DR5 |
| linear addr. | reserved | reserved |
| DR6 | DR7 | |
| breakpoint status | breakpoint trigger | |

## Model-/machine-specific registers (MSR):

| | |
|---|---|
| TSC (64-bit) | IA32_TIME_STAMP_COUNTER |
| Enable Misc. Features (SpeedStep, XD, etc.) | IA32_MISC_ENABLE |
| Enable Extd. Features (Long mode, etc.) | IA32_EFER |
| ⋮ | |
| CS target for CPL0 | IA32_SYSENTER_CS |
| CPL0 code entry point | IA32_SYSENTER_EIP |
| Stack pointer for CPL0 | IA32_SYSENTER_ESP |

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## Memory Management:

| | | | |
|---|---|---|---|
| | GDTR | base | limit |
| seg-sel | LDTR | base | limit |
| | IDTR | base | limit |
| seg-sel | TR | base | limit |

15 ... 0 63 ..... 0 31 ..... 16

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ID | VIP | VIF | AC | VM | RF | 0 | NT 1 | IOPL 1 | 1 | OF | DF | IF | TF | SF | ZF | 0 | AF | 0 | PF | 1 | CF |

## SSE – Streaming SIMD Extensions, AVX – Advanced Vector Extensions:

added for SSE

MXCSR — Control- and status register

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XMM0 . . . XMM7: SSE-128 registers

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| float3 | | | | float2 | | | | float1 | | | | float0 | | | |
| double1 | | | | | | | | double0 | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| w7 | | w6 | | w5 | | w4 | | w3 | | w2 | | w1 | | w0 | |
| dword3 | | | | dword2 | | | | dword1 | | | | dword0 | | | |
| qword1 | | | | | | | | qword0 | | | | | | | |
| 128-bit double quadword | | | | | | | | | | | | | | | |

32-bit float
64-bit double
XMM0..7
8..128-bit int

added for AVX

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| float7 | float6 | float5 | float4 | float3 | float2 | float1 | float0 |
| double3 | | double2 | | double1 | | double0 | |

YMM0

YMM0 . . . YMM15: AVX-256 registers (lower 128 bits: XMM0 . . . XMM15)

⋮

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| float7 | float6 | float5 | float4 | float3 | float2 | float1 | float0 |
| double3 | | double2 | | double1 | | double0 | |

YMM15

… (MMX-) integer registers … floating-point registers (double-prec.) … floating-point registers (single-prec.)
… only available in 64-bit (long) mode … not accessible at the same time as AH, BH, CH, DH (require REX prefix)
**(Mostly) managed by the OS:** … segment, status- and control registers … system registers